AMENDMENTS IN THE CLAIMS

Please amend the claims as indicated below. The language being added is underlined ("___") and the language being deleted contains strikethrough ("—"):

1. (Original) A substrate adapted for use in integrated circuits, the substrate comprising:

a first substrate layer comprising an organic material;

a first conductor layer fabricated on an upper surface of the first substrate layer; and

an integrated inductor fabricated on an upper surface of the first conductor layer.

2. (Canceled)

3. (Original) The substrate of claim 1, wherein the integrated inductor comprises a microstrip loop inductor.

4. (Original) The substrate of claim 1, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

5. (Original) The substrate of claim 1, further comprising a second conductor layer fabricated on a lower surface of the first substrate layer, the second conductor layer adapted as a ground plane for the first conductor layer.

6. - 7. (Canceled)

8. (Original) The substrate of claim 1, further comprising a second conductor layer fabricated on a lower surface of the first substrate layer, wherein two points of the integrated inductor are electrically connected through a via connected to the second conductor layer.

9. (Original) The substrate of claim 8, further comprising:

a second substrate layer fabricated on a lower surface of the second conductor layer; and

a third conductor layer fabricated on a lower surface of the second substrate layer.

10. (Original) The substrate of claim 9, wherein the second substrate layer comprises an organic material.

11. (Original) The substrate of claim 10, wherein the organic material is at least one of an epoxy-based material and a liquid crystalline polymer.

12. - 44. (Canceled)

45. (Original) A substrate adapted for use in integrated circuits, the substrate comprising:

a first substrate layer;

a first conductor layer fabricated on an upper surface of the first substrate layer; and

an integrated inductor fabricated on an upper surface of the first conductor layer, the integrated inductor comprising a microstrip loop inductor.

46. (Original) The substrate of claim 45, wherein the configuration of the microstrip loop inductor is designed to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

47. (Original) The substrate of claim 45, wherein the number of loops and the line width of the microstrip loop inductor are designed to optimize at least one of a frequency for a maximum Q factor, an effective inductance, and a self resonant frequency.

48. (Original) The substrate of claim 45, wherein the microstrip loop inductor comprises a single loop having a line width of approximately 2 mils and an area of approximately 3.5 millimeters^2.

49. (Original) The substrate of claim 48, wherein the microstrip loop inductor has an effective inductance of approximately 7.7 nH, a maximum Q factor of approximately 90 at approximately 2.4 GHz, and a self resonating frequency of approximately 7.2 GHz.

50. - 125. (Canceled)